IN THE DRAWINGS

As described below, the Specification was amended to reference elements 17 and 18 as correctly shown in FIG. 6, With this amendment to the Specification, the Applicants respectfully submit that the originally filed drawings comply with 37 CFR 1.84(p)5 and the Examiner's rejection should be withdrawn.

REMARKS

Applicants have studied the Office Action dated May 23, 2005, and Claim 19 has been amended for grammatical purposes only. No new matter was added. Claims 1-19 remain pending in the application. Reconsideration and allowance of the pending claims in view of the following remarks and arguments are respectfully requested. Applicants submit that the application is in condition for allowance. In the Office Action, the Examiner:

- Objected to the drawings as failing to particularly comply with 37 C.F.R. 1.84(p)5 because they include the following reference characters not mentioned in the description: elements 17 and 18;
- Objected to the disclosure because of minor informalities;
- Objected to claim 19 because "nanometers" appears in the claim;
- Rejected claims 1-4, 13-14, and 18 under 35 U.S.C. § 102(b) as being anticipated by Subramanian et al. (U.S. Patent No. 6,348,406);
- Rejected claims 5-6 under 35 U.S.C. § 103(a) as being unpatentable over Subramanian et al. (U.S. Patent No. 6,348,406) in view of Tanaka et al. (U.S. Patent Publication No. 2003/0165750);
- Rejected claims 9-12 under 35 U.S.C. § 103(a) as being unpatentable over Subramanian et al. (U.S. Patent No. 6,348,406) in view of S. Wolf "Silicon Processing for the VLSI Era", Vol. 1; and
- Rejected claims 8, 15, 16, 17, and 19 under 35 U.S.C. § 103(a) as being unpatentable over Subramanian et al. (U.S. Patent No. 6,348,406).

Overview of the Present Invention

The present invention provides a production process for a flash memory. EPROM memories with floating grill are programmable electrically, but are not erasable electrically. These memories are erasable only by ultraviolet rays. EPROM memories are programmed by using the phenomenon of thermal agitation in the conduction channel under the effect of conventional saturation. This phenomenon is irreversible.

EEPROM memories are programmable and erasable electrically. EEPROM memories are programmed or erased via tunnel effect. Internal memory circuits, such as charge pumps or multipliers, usually produce programming and erasing voltages. Flash memories are components formed by a matrix of memory cells, each having a transistor with floating gate. In conventional terms, it is possible to individually program each cell of the matrix, but the data must be erased for a block of cells. Each cell is usually formed from a source, a drain, a floating gate and a control cell. The transistors with floating gate of the matrix are arranged in rows. Forming a source line connects the sources of the transistors of a row. Hot carriers of the drain program the cell. The cell is erased by tunnel effect.

The production process for certain flash memories utilizes an etching step known as forming an auto-aligned or SAS source (Self-Aligned Source). The SAS etching digs out source lines in the substrate on which the flash memory is formed. During a subsequent stage of the process, arsenic is implanted at high concentration in the etched zone to form the source line of the transistors with floating gate. Although useful, Flash memories have disadvantages. One disadvantage is that the time required to erase flash memories is considerable, thus limiting their fields of application.

The present invention overcomes the problems with the prior art by reducing the time needed to erase a flash memory. For this, polymers deposited under the cell during the attack of a protective resin of the cells are removed during the etching stage of the auto-aligned source. The source line is then implanted in the etched zone. More specifically, the present invention provides a method for producing a flash memory comprising forming at least two adjacent rows of precursor stacks of floating gate transistors on a semiconductor substrate. The precursor stacks being at least partially covered by a protective resin and being separated by a formation zone for a source line. Forming a trench in the formation zone for the source line by an attack of the formation zone and of the protective resin so as to result in a deposit of residue

from the protective resin below the precursor stacks. Removing the deposit of residue and implanting a source line in the formation zone below the precursor stacks.

Objection to the Drawings

The Applicants have amended the Specification to properly reference elements 17 and 18 as shown in FIG. 6. No new matter has been added. The Applicants respectfully submit that the objection to the drawings has been overcome and should be withdrawn/

Objection to the Specification

The Applicants have corrected typographical errors in paragraph [007] and [0032]. The Applicants believe that the objection of the Specification has been overcome and request withdrawal of the objection.

Objection to Claim 19

Claim 19 has been amended to recite "nanometers" instead of "nanometres". This amendment was for clarification purposes only independent of patentability. This amendment does not narrow the scope of claim 19 within the meaning of Festo.[1] The Applicants believe the objection to claim 19 has been overcome and respectfully request withdrawal of the objection.

Rejection under 35 U.S.C. §102(b) as being anticipated by Subramanian

As noted above, the Examiner rejected claims 1-4, 13-14, and 18 under 35 U.S.C. § 102(b) as being anticipated by Subramanian et al. (U.S. Patent No. 6,348,406). This rejection is respectfully traversed.

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[1] Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co., Ltd., No. 00-1543 (122 S. Ct. 1831; 2002 U.S. LEXIS 3818; 62 U.S.P.Q.2D (BNA) 1705)(Decided May 28, 2002).

Referring to claim 1, the Examiner at page 5 of the office action states that Subramanian discloses "*a method for producing a flash memory comprising:*

forming at least two adjacent rows of precursor stacks of floating gate transistors 214 on a semiconductor substrate 102, with the precursor stacks 210 being at least partially covered by a protective resin 212 & 318 and being separated by a formation zone for a source line 202;

forming a trench 202 in the formation zone for the source line 202 by an attack of the formation zone and of the protective resin 212 & 318 so as to result in a deposit of residue from the protective resin below the precursor stacks (Column 7 lines 26-29, please noet the claim 1 directly refers to self-aligned source etching process;

removing the deposit of residue (column 2 lines 30-34); and

implanting a source line 202 in the formation zone below the precursor stacks (column 7 lines 36-52, please note Subramanian teaches to form source and common line CS)".

However, the Applicants respectfully disagree with the Examiner's characterization of Subramanian. First of all, Subramanian is completely silent on "an attack of the formation zone and of the protective resin so as to result in a deposit of residue from the protective resin below the precursor stacks" as recited for claim 1.

Nowhere does Subramanian teach an attack of a material located under the precursor stack or the presence of a residue from a previous attack. As shown by the FIGs. 2 and 3 of the present invention below, the formation zone and the protective resin 14 are attacked resulting in a deposit of residue 15 from the protective resin 14 below the precursor stacks 31, 32.

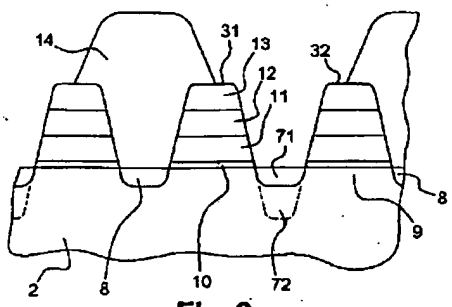

Fig. 2

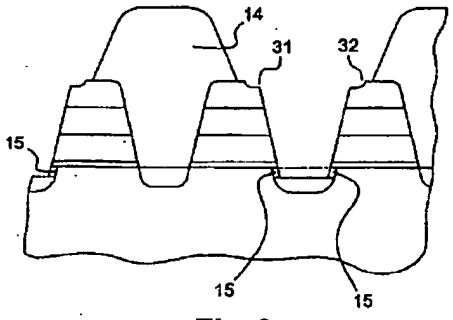

Fig. 3

Nowhere does Subramanian teach a deposit of residue 15. Column 7, lines 26-29 of Subramanian cited by the Examiner merely state that the portions of the field oxide regions and the gate dielectric layer between every second pair of adjacent stacked gate structures in the array core are typically removed in preparation for the formation of the common line CS. This is not the same as "an attack of the formation zone and of the protective resin so as to result in a deposit of residue from the protective resin below the precursor stacks", as recited for claim 1. Accordingly, the present invention distinguishes over Subramanian for at least this reason.

Furthermore, the Examiner included the following figures 2C and 6 from Subramanian to further support the rejections of claims 1-2, 13-14, and 18.

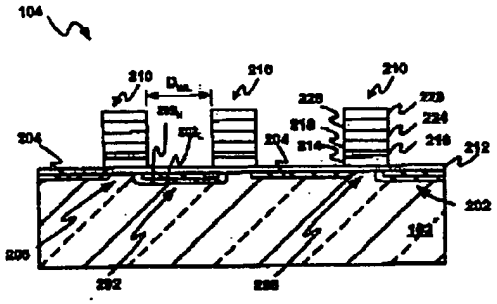

FIG. 2C (PRIOR ART)

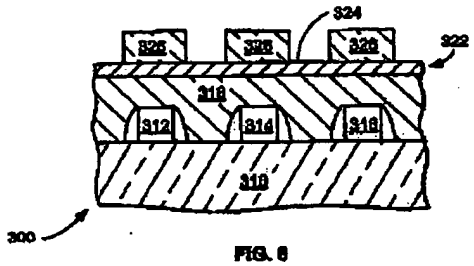

FIG. 6

The Examiner points to elements 212 of FIG. 2C and element 318 of FIG. 6 in Subramanian and compares them to the protective resin 14 of the present invention, which is illustrated in FIG. 2 and FIG 3 above. As stated above, Subramanian explicitly teaches that element 212 and 318 are dielectric layers, not protective resins as recited in the claimed invention. Additionally, FIG. 2C of Subramanian teaches that the dielectric layer, which is part of the stacked gate structure 210 (See column 5, lines 39-40), is first deposited then the stacks 210 and the layers of the stack 210 are formed. For example, Subramanian teaches at column 6, lines 31-37 that the dielectric layer 212 is initially formed on the substrate 102 then a layer of conductive polysilicon is formed on top of the dielectric layer 212. Additional layers are then added.

The dielectric layer 212 of Subramanian is below the stack 210; however, this layer is deposited on the substrate before any of the other layers of the stack 210 are deposited. The present invention, on the other hand, recites "an attack of the formation zone and of the protective resin so as to result in a deposit of residue from the protective resin below the precursor stacks". In other words, the precursor stacks are already in place when the residue is deposited below the precursor stacks.

Furthermore, layer 318 is not at any point formed below precursor stacks. Layer 318, which is a dielectric layer, is below an ARC layer 322, which is below a photoresist 326, not a precursor stack. Accordingly, the present invention distinguishes over Subramanian for at least these reasons as well.

Additionally, as stated briefly above, the Examiner compares element 212 of FIG. 2C and element 318 of FIG. 6 of Subramanian to the protective resin 14 of the present invention. The Applicants respectfully point out that element 212 of FIG. 2C and element 318 of FIG. 6 of Subramanian are not the same as the protective layer 14 of the present invention. Elements 212 and 318 of Subramanian are dielectric layers. See column 7, lines 24-25 and lines 59-60 of Subramanian.

In contrast, paragraph [0031] of the present invention states:

> *The precursor stacks are at least partially covered in a layer of protective resin 14, forming a mask for the subsequent stages of SAS etching and implantation of the source lines. A thick DUV or i-line resin can specially be used as protective resin. The protective resin has sufficient thickness to avoid implantation in the precursor stacks during formation of the source line.*

Accordingly, the present invention distinguishes over Subramanian for at least this reason as well.

Also, nowhere does Subramanian teach "removing the deposit of residue", as recited for claim 1. The Examiner directs the Applicants to column 2, lines 30-34, wherein Subramanian only teaches an "attack" of the conductive material patterning the source and drain conductive contacts. This step cannot remove any deposit of residue since the step is performed after the metal deposit on the contact zones. Accordingly, the present invention distinguishes from Subramanian for at least this reason as well.

Furthermore, column 7, lines 36-53 cited by the Examiner is support of the Examiner's assertion that Subramanian teaches "implanting a source line in the formation zone below the precursor stacks" merely mentions a classical doping for the source and drain zones. Although this doping may extend under the stack, nowhere does Subramanian teach the presence or removal of residue, as recited for the present invention. Accordingly, the present invention distinguishes over Subramanian for at least this reason as well.

The Examiner cites 35 U.S.C. § 102(b) and a proper rejection requires that a single reference teach (i.e., identically describe) each and every element of the rejected

claims as being anticipated by Subramanian.[2] Because the elements in independent claim 1 of "...the precursor stacks being at least partially covered by a protective resin and being separated by a formation zone for a source line; forming a trench in the formation zone for the source line by an attack of the formation zone and of the protective resin so as to result in a deposit of residue from the protective resin below the precursor stacks; removing the deposit of residue..." is not taught or disclosed by Subramanian, Subramanian does not identically describe each and every element of claim 1. Accordingly, claim 1 distinguishes over Subramanian for at least these reasons. The Applicants respectfully submit that the Examiner's rejection under 35 U.S.C. § 102(b) has been overcome and the rejection should be withdrawn.

For the foregoing reasons, independent claim 1 distinguishes over Subramanian. Claims 2-4, 13-14, and 18 depend from claim 1. Since dependent claims contain all the limitations of the independent claims, claims 2-4, 13-14, and 18 distinguish over Subramanian, as well, and the Examiner's rejection should be withdrawn. However, additional remarks regarding claims 3-4 and 13-14 are given below.

Referring to claim 3, the Examiner states on page 6 of the office action that Subramanian discloses *"the method of claim 1, wherein the forming of a trench 202 includes forming a trench so as to result in the protective resin 212 & 318 formed from a thick DUV resin 322 (Column 8 lines 18-27, also note Anti-reflective coating (ARC) layer*

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[2] See MPEP §2131 (Emphasis Added) "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim."

is typically a polymer film, which is highly absorbing and non-bleaching at the exposure wavelengths associated with the photolithographic process)"

As discussed above, layers 212 & 318 are dielectric layers and column 8, lines 18-27 merely teach that an ARC layer 322 is used as the mask for forming the contacts or local interconnects. The present invention, on the other hand recites "wherein the forming a trench includes forming a trench so as to result in the protective resin formed from a thick DUV resin". Paragraph [0031] of the present invention states "a thick DUV or i-line resin can specially be used as protective resin". Layers 212 and 318 in Subramanian are two distinct layers from layer 322 and are not formed from layer 322. Therefore, Subramanian does not teach, anticipate, or suggest "wherein the forming a trench includes forming a trench so as to result in the protective resin formed from a thick DUV resin".

Referring to claims 13 and 14, the Examiner on page 7 of the office action states that Subramanian discloses "*removing the protective resin 212 following implantation of the source line 202*". However, the Examiner does not point to any specific place or general place for that matter in Subramanian to support the Examiner's assertion that Subramanian teaches this element of claims 13 and 14. Therefore, the rejection of claims 13 and 14 is improper and the rejection should be withdrawn.

Furthermore, the Examiner states that layers 212 and 318 are the same as the protective resin 14 in the present invention. Therefore, Subramanian would have to teach that layers 212 and 318, which are dielectric layers, are removed after implantation of the source line. As can be clearly seen from FIG. 2C, the source line exists and the layer 212 also exists. Accordingly, Subramanian does not teach, anticipate or suggest "removing the protective resin following implantation of the source line".

Rejections under 35 U.S.C. §103(a) in view of Subramanian and Tanaka

As noted above, the Examiner rejected claims 5-6 under 35 U.S.C. § 103(a) as being unpatentable over Subramanian et al. (U.S. Patent No. 6,348,406) in view of Tanaka et al. (U.S. Patent Publication No. 2003/0165750).

Claims 5-6 depend from independent claim 1. Since dependent claims contain all the limitations of independent claims, claims 5-6 also distinguish over Subramanian for the reasons above, which will not be repeated here.

As the Examiner correctly stated on page 8 of the office action, Subramanian does not disclose "*wherein forming of the trench 202 includes forming a trench so as to result in the protective resin formed of thick I-line resin*". The Examiner goes on to combine Subramanian with Tanaka stating that Tanaka teaches "*wherein forming of the trench 202 includes forming a trench so as to result in the protective resin formed of thick I-line resin (column 6 lines 48-54)*".[3]

Tanaka teaches a method of manufacturing an electronic device. Nowhere does Tanaka teach, anticipate, or suggest "...the precursor stacks being at least partially covered by a protective resin and being separated by a formation zone for a source line; forming a trench in the formation zone for the source line by an attack of the formation zone and of the protective resin so as to result in a deposit of residue from the protective resin below the precursor stacks; removing the deposit of residue...".

Accordingly, the limitations taken "as a whole" in claim 1 are not present in Subramanian taken alone or in view of Tanaka. Claim 1, therefore, distinguishes over Subramanian taken alone and/or in combination with Tanaka for at least this reason.

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[3] Applicants make no statement whether such combination is even proper.

Further, when there is no suggestion or teaching in the prior art for "...the precursor stacks being at least partially covered by a protective resin and being separated by a formation zone for a source line; forming a trench in the formation zone for the source line by an attack of the formation zone and of the protective resin so as to result in a deposit of residue from the protective resin below the precursor stacks; removing the deposit of residue..." the suggestion cannot come from the Applicants' own specification. The Federal Circuit has repeatedly warned against using the Applicant's disclosure as a blueprint to reconstruct the claimed invention out of isolated teachings of the prior art. See MPEP §2143 and Grain Processing Corp. v. American Maize-Products, 840 F.2d 902, 907, 5 USPQ2d 1788 1792 (Fed. Cir. 1988) and In re Fitch, 972 F.2d 160, 12 USPQ2d 1780, 1783-84 (Fed. Cir. 1992).

For the foregoing reasons, independent claim 1 distinguishes over Subramanian taken alone and/or in view of Tanaka. Claims 5-6 depend from claim 1. Since dependent claims contain all the limitations of the independent claims, claims 5-6 distinguish over Subramanian taken alone and/or in view of Tanaka, as well, and the Examiner's rejection should be withdrawn.

Rejections under 35 U.S.C. §103(a) in view of Subramanian and S. Wolf

As noted above, the Examiner rejected claims 9-12 under 35 U.S.C. § 103(a) as being unpatentable over Subramanian et al. (U.S. Patent No. 6,348,406) in view of S. Wolf "Silicon Processing for the VLSI Era", Vol. 1.

Claims 9-12 depend from independent claims 1. Since dependent claims contain all the limitation of independent claims, claims 9-12 also distinguish over Subramanian for the reasons above, which will not be repeated here.

As the Examiner correctly stated on page 9 of the office action, Subramanian does not teach "*the removing of the deposit of residue includes removing the deposit of residue by generating dioxygen plasma*". However, the Examiner went on to combine Subramanian with S. Wolf stating that S. Wolf teaches "*removing of the deposit of residue includes removing the deposit of residue by generating dioxygen plasma*".[4]

Nowhere does S. Wolf teach a protective resin that is attacked resulting in a deposit of residue from the protective resin below precursor stacks, as recited for claim 1. Accordingly, S. Wolf is completely silent on "...the precursor stacks being at least partially covered by a protective resin and being separated by a formation zone for a source line; forming a trench in the formation zone for the source line by an attack of the formation zone and of the protective resin so as to result in a deposit of residue from the protective resin below the precursor stacks; removing the deposit of residue..." and the present invention distinguishes fro S. Wolf for at least this reason.

Therefore, the limitations taken "as a whole" in claim 1 are not present in Subramanian taken alone or in view of S. Wolf and claim 1 distinguishes over Subramanian taken alone and/or in combination with S. Wolf for at least this reason.

Further, when there is no suggestion or teaching in the prior art for "...the precursor stacks being at least partially covered by a protective resin and being separated by a formation zone for a source line; forming a trench in the formation zone for the source line by an attack of the formation zone and of the protective resin so as to result in a deposit of residue from the protective resin below the precursor stacks; removing the deposit of residue..." the suggestion cannot come from the Applicants' own specification. The Federal Circuit has repeatedly warned against using the Applicant's

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[4]Applicants make no statement whether such combination is even proper.

disclosure as a blueprint to reconstruct the claimed invention out of isolated teachings of the prior art. See MPEP §2143 and Grain Processing Corp. v. American Maize-Products, 840 F.2d 902, 907, 5 USPQ2d 1788 1792 (Fed. Cir. 1988) and In re Fitch, 972 F.2d 160, 12 USPQ2d 1780, 1783-84 (Fed. Cir. 1992).

For the foregoing reasons, independent claim 1 distinguishes over Subramanian taken alone and/or in view of S. Wolf. Claims 9-12 depend from claim 1. Since dependent claims contain all the limitations of the independent claims, claims 9-12 distinguish over Subramanian taken alone and/or in view of S. Wolf, as well, and the Examiner's rejection should be withdrawn.

Rejections under 35 U.S.C. §103(a) in view of Subramanian

As noted above, the Examiner rejected claims 8, 15, 16, 17, and 19 under 35 U.S.C. § 103(a) as being unpatentable over Subramanian et al. (U.S. Patent No. 6,348,406).

Referring to claim 8, the Examiner states that Subramanian discloses "*the method of claim 6, wherein the forming at least two adjacent rows of precursor stacks of floating gate transistors 210 on a semiconductor substrate 102 includes forming a semiconductor substrate with a drain 204 for each precursor stack, wherein the drain is covered in a resin 212 & 318; and wherein for each of the precursor stacks, the drain 204, is formed opposite the formation zone for the source line 202*".

However, as stated above with respect to claim 1, Subramanian does not teach, anticipate, or suggest "...the precursor stacks being at least partially covered by a protective resin and being separated by a formation zone for a source line; forming a trench in the formation zone for the source line by an attack of the formation zone and of the protective resin so as to result in a deposit of residue from the protective resin below the precursor stacks; removing the deposit of residue..." and the present invention distinguishes over Subramanian for at least this reason as well.

Referring to claims 15-17, the Examiner on page 11 states that Subramanian discloses "*removing the protective resin 212 following the implantation of the source line 202*". However, as stated above for claims 13 and 14, the Examiner does not point to any specific place or general place for that matter in Subramanian to support the Examiner's assertion. Therefore, the rejection of claims 15-17 is improper and the rejection should be withdrawn.

Furthermore, the Examiner states that layers 212 and 318 are the same as the protective resin 14 in the present invention. Therefore, Subramanian would have to teach that layers 212 and 318, which are dielectric layers, are removed after implantation of the source line. As can be clearly seem from FIG. 2C, the source line exists and the layer 212 also exits. Additionally, the remarks and arguments made above with respect to claim 1 are applicable here and will not be repeated. Therefore, the present invention distinguishes over Subramanian for at least these reasons as well.

Referring to claim 19, the Examiner on page 12 states that Subramanian discloses "*wherein the implanting the source line includes implanting the source line 25 nanometres out from an edge under a gate oxide of the precursor stacks*". The Examiner goes on to state

> *given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved. See in re Aller, Lacey and Hall (10 USPQ 233-237) 'It is not inventive to discover optimum or workable ranges by routine experimentation'. Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions*

or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodru; 919 f 2d 1575, 1578, 16 USPD2d 1934, 1936 (Fed. Cir. 1990).

The remarks and arguments made above with respect to claim 1 are applicable here and will not be repeated. Therefore, Subramanian does not teach, anticipate, or suggest "...the precursor stacks being at least partially covered by a protective resin and being separated by a formation zone for a source line; forming a trench in the formation zone for the source line by an attack of the formation zone and of the protective resin so as to result in a deposit of residue from the protective resin below the precursor stacks; removing the deposit of residue..." and the present invention distinguishes over Subramanian for at least this reason as well.

Moreover, the Federal Circuit has consistently held that when a §103 rejection is based upon a modification of a reference that destroys the intent, purpose or function of the invention disclosed in the reference, such a proposed modification is not proper and the *prima facie* case of obviousness can not be properly made. See In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984).

Here the intent, purpose and function of Subramanian is forming a dielectric layer 212, 318 on the substrate before any of the other layers of the stack 210 are deposited. See Subramanian at col. 6, lines 31-37. The intent of the present invention, on the other hand, is to at least partially cover precursor stacks with a protective resin and attacking the formation zone and of the protective resin so as to result in a deposit of residue from the protective resin below the precursor stacks; removing the deposit of residue. In other words, the precursor stacks are already deposited when the protective resin is deposited. Therefore, the modification of Subramanian needed to accomplish the present invention destroys the intent and purpose of

Subramanian and results in an inoperable system. Accordingly, the Examiner's case of *"Prima Facie Obviousness"* should be withdrawn.

For the foregoing reasons, independent claim 1 distinguishes over Subramanian. Since dependent claims contain all the limitations of the independent claims, claims 8, 15-17, and 19 distinguish over Subramanian and the Examiner's rejection should be withdrawn.

CONCLUSION

In this Response, Applicants have amended certain claims. In light of the Office Action, Applicants believe these amendments serve a useful clarification purpose, and are desirable for clarification purposes, independent of patentability. Accordingly, Applicants respectfully submit that the claim amendments do not limit the range of any permissible equivalents.

Applicants acknowledge the continuing duty of candor and good faith to disclosure of information known to be material to the examination of this application. In accordance with 37 CFR § 1.56, all such information is dutifully made of record. The foreseeable equivalents of any territory surrendered by amendment is limited to the territory taught by the information of record. No other territory afforded by the doctrine of equivalents is knowingly surrendered and everything else is unforeseeable at the time of this amendment by the Applicants and their attorneys.

Applicants respectfully submit that all of the grounds for rejection stated in the Examiner's Office Action have been overcome, and that all claims in the application are allowable. No Previously Presented matter has been added. It is believed that the application is now in condition for allowance, which allowance is respectfully requested.

PLEASE CALL the undersigned if that would expedite the prosecution of this application.

Respectfully Submitted,

Date: August 23, 2005

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